REMARKS

Claims 1-19 are pending in the current application. In an Office Action dated July 14, 2006 ("Office Action"), the Examiner rejected claims 1-19 under 35 U.S.C. § 101. Applicant respectfully traverses these rejections.

Applicant's representative has amended independent claims 1, 10, and 19 to more particularly point out and distinctly claim that which Applicant considers to be the invention. In particular, judging from the Examiner's 35 U.S.C. § 101 rejections, it appears that the original claims did not sufficiently clearly state that the current claims are directed to a fast and efficient computer-executed operation - namely a multiply-and-add *computer* operation.

The Examiner's stated rejections do not appear to be consistent either with the "Interim Guidelines for Examination of Patent Examination of Patent Applications for Patent Subject Matter Eligibility" or with current case law. As one example, the Examiner states: "Therefore, the claimed invention is directed to non-statutory subject matter as the claims fail to assert a practical application to the invention." As pointed out in section II(A) of the "Interim Guidelines for Examination of Patent Examination of Patent Applications for Patent Subject Matter Eligibility," it is not the claims, but the disclosure that "should contain some indication of the practical application of the claimed invention." Applicant clearly points out the deficiencies in modern computer systems with respect to multiple-precision multiply-and-add operations, in the paragraph beginning on line 22 of page 3. On lines 16-18, Applicant states that a straightforward implementation of a multiple-precision multiply-and-add operation is not amendable to instruction-execution parallelism, and is inefficient. On lines 3-7 of page 17 of the current application, Applicant discusses, in detail, the greater efficiency and elimination of write dependencies that characterizes a described, multiple-precision multiply-and-add-operation embodiment of the present invention. Thus, the current application provides numerous, very detailed indications of the utility of the present invention, as required by section II(A) of the "Interim Guidelines for Examination of Patent Examination of Patent Applications for Patent Subject Matter Eligibility." As another

example, neither the "Interim Guidelines for Examination of Patent Examination of Patent Applications for Patent Subject Matter Eligibility" nor *State Street* require that an invention physically transform a computer system or that an invention result in a physical transformation, although, in fact, a multiple-precision multiply-and-add operation does result in transformation of the physical state of a number of computer-system registers, as clearly claimed in claim 1 by the language "and stores results of the multiply-and-add instructions as intermediate results." Storing of values in a computer system necessarily involves a physical transformation. But, currently, in Applicant's representative's understanding, it is the usefulness of an invention that needs to be demonstrated, and patentability is not determined by whether or not a physical transformation occurs.

Increasing the speed and efficiency of basic computer operations is a fundamental goal of much of research and development efforts in computer science and electronics. In fact, computer systems are commonly evaluated and characterized by the speed by which they execute floating-point multiplication operations. Computers, compilers, and many other fundamental components of computer systems operate to transform input numbers to output numbers, generally storing the output values, at least temporarily, in an electronic memory. For example, compilers merely transform one set of numbers, a binary encoded high-level program, into another set of numbers, a binary-encoded machine-code version of the program. A simple search of the USPTO issued-patent database will reveal many hundreds of patents issued on patent applications directed to compilers and compiler improvements, including a number of issued patents prepared and prosecuted by Applicants' representative, including U.S. Patent No. 6,182,284 B1 and U.S. Patent No. 6,260,190 B1. Computer processors simply transform input numbers to output numbers, and computer processors are also definitely patentable. A claimed invention that improves the performance of a computer system by providing a faster and more efficient multiple-precision multiply-and-add operation that increases the speed and efficiency by which the computer system can perform any task involving multiple-precision arithmetic, including almost all scientific and engineering application programs, image-rendering application programs, and many other application programs, is clearly both useful and patentable.

In Applicant's representative's opinion, all of the claims remaining in the current application are clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,
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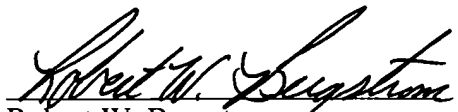

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